Tailor-Made for Efficiency:
Ultra-Low Power Implementation Flow

ChipEx2024, Tel Aviv, Israel May 7, 2024

ChipEx2024

HELLO!

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Avnet ASIC Israel

AGENDA

- Introduction
- 4nm technology adaptation and challenges
- Early RTL exploration
- PnR flow
- Power estimation
- Power grid
- Post-Si measurements

WHO WE ARE

Avnet ASIC Israel

- Your partner for ASIC design & Turnkey manufacturing
- Offering flexible solutions & business models
- Full range of ASIC services (down to 4nm EUV, 3nm WIP) from specification to mass production, with robust design practices & smooth ramp-up to mass production
- In-house RISC-V CPU family and HW security modules
- Strong in-house productization capabilities (testers, handler)
- TSMC VCA Partner – silicon channel for customers

AVNET Reach Further™

All services under one roof

35 years of experience

Hundreds of successfully completed projects

WHO WE ARE

Blockstream Israel

- Blockstream is a leading provider of blockchain technologies and remains on the forefront of work in cryptography and distributed systems
- Blockstream Israel, the corporate ASIC division, is a trailblazer in the Bitcoin arena, aiming to accelerate Bitcoin mining capabilities
- We are in a mission to launch the world's first enterprise-class miner
- Leveraging the unparalleled security of Bitcoin, we construct crypto-financial frameworks aimed at enhancing market efficiency and reducing reliance on trust

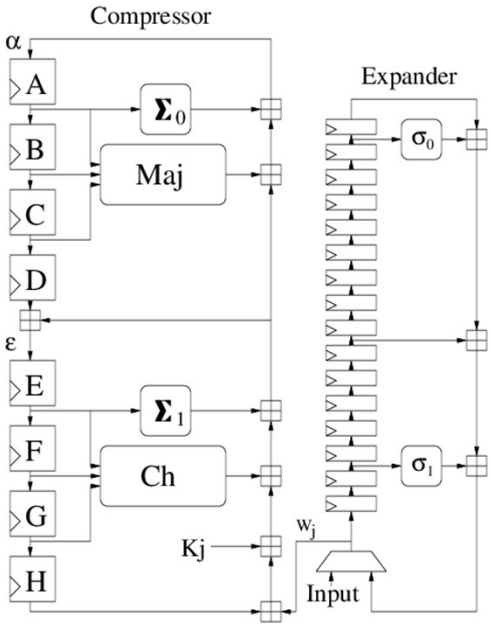
KEY DECISIONS IN ASIC DESIGN

- Foundry (fabless companies)
- Tech node
- Libraries- HS/HD/VTs
- Memory Compiler
- Operating Voltage
- Frequency
- Power budget

ASIC DESIGN FOR BLOCKCHAIN APPLICATION

Implementation of DSHA-256 hashing algorithm:

- Pure Stdcell
- Hash power vs. power consumption
- Number of engines: area vs. performance
- Arithmetic logic susceptible to glitches
- Substantial dynamic power



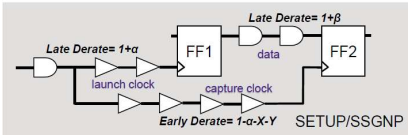
ASIC DESIGN FOR BLOCKCHAIN APPLICATION

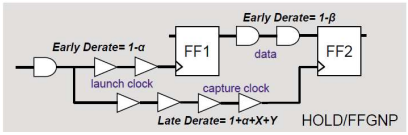
Dynamic power analysis: $P_{dyn} = \alpha f C V^2$

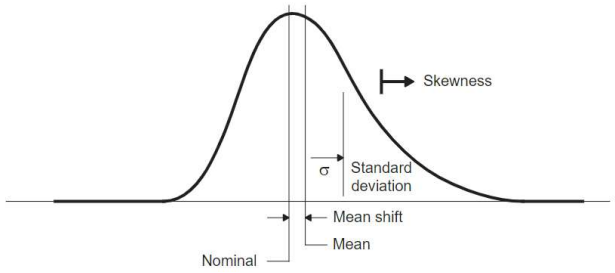
Parameter	*Power Dependency*	*Approach*
activity factor	linear	architecture, algorithm optimization
frequency	linear	advanced node, custom design
capacitance	linear	advanced node, custom design
voltage	quadratic	lower operating voltage (usage of ulvt/elvt cells)

TECHNOLOGY ADOPTION

- TSMC N4P improves both density (~1.08x) and power (~13% at same speed) compared to N5
- Ultra-Low Vt and Extreme-Low Vt cell types selected
- Significantly slow transistors at low temperature
- Special signoff conditions: extended hold constraint (μ+3σ), moment-based asymmetric delay distribution, voltage and temperature margin, wire ocv, spatial ocv
- Additional placement limitations







RE-CHARACTERIZATION CHALLENGES

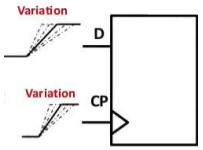
- Further optimization by re-characterization of TSMC N4P for low voltage ($< \frac{std\ Volt.}{2} \pm 10\%$) within application typical temperature range

- Innovative initiatives often come with a price- special flow is required near threshold when $V_t + 50mV \leq VDD \leq V_t + 125mV$:

  - additional σ for hold constraint variation (i.e, μ+**4**σ)
  - wider range for transition variation:

  data transition: μ+2σ

  clock transition: μ+3σ

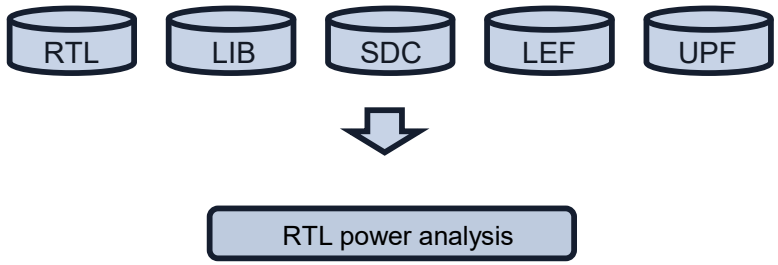
  

  - CRPR sigma removal is disabled in min-pulse-width check
  - considering input transition variation impact on constraint variation

- Slow corner delays are 10x higher than fast

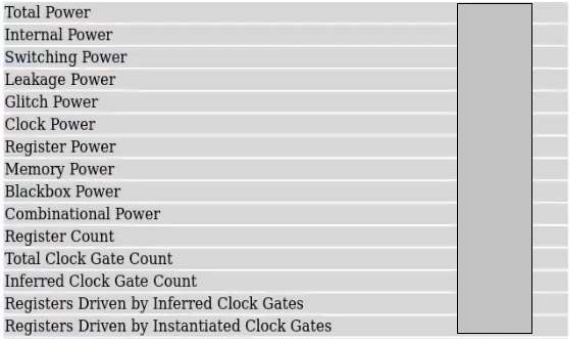
EARLY FEEDBACK

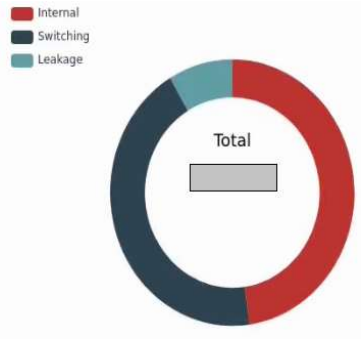
- Early RTL exploration facilitated PPA optimization, providing quick feedback before physical implementation flow completes
- A predictive synthesis engine was used to perform reliable power analysis using minimal set of collaterals, enabling short TAT and feedback on custom cells contribution



EARLY FEEDBACK

- Deviation between RTL exploration and power signoff tool (SDF based GLS):
  - Net Switching Power: 0.8%
  - Cell Internal Power: 0.4%
  - Cell Leakage Power: 16%



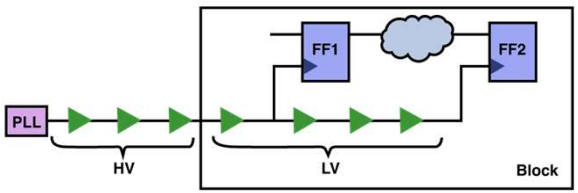


- Deviation between RTL exploration and PnR tool (route stage):
  - Cell Count: 4%
  - Cell Area: 6%

- Runtime is ~4x faster (initOpto)

CLOCK TREE

- Optimized clock tree, constructed using extreme-low-Vt cells, minimizes the exceptional OCV effects, ensuring low latency
- Clock routing uses triple spacing as needed, serving as a place-holder for incremental fixes (coaxial shielding)
- Main clock tree branches are activated in higher voltage, local branches- in low voltage

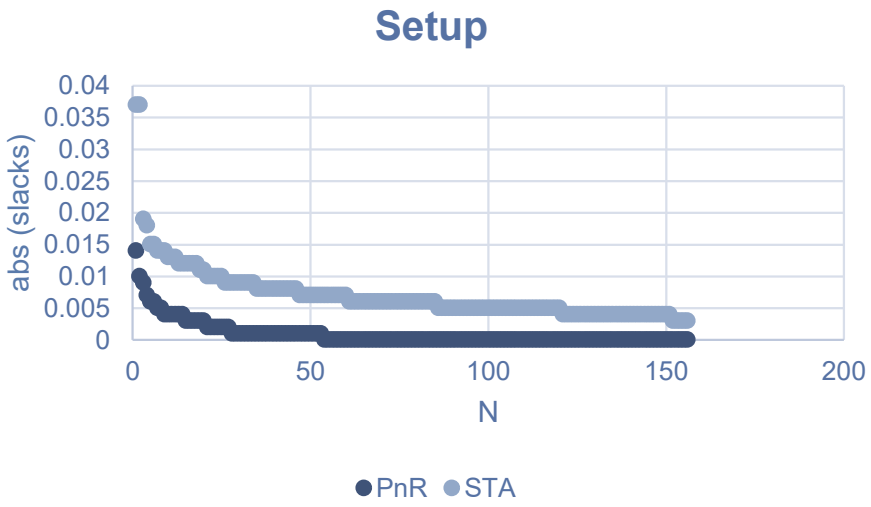


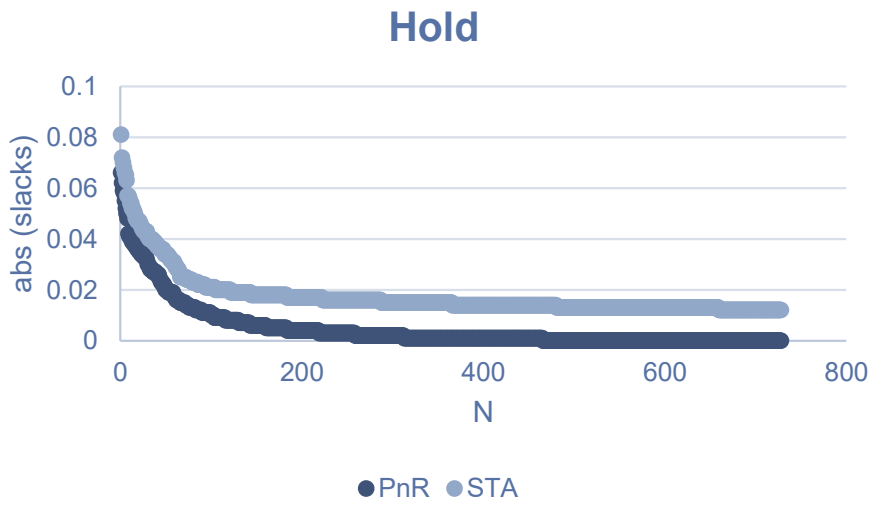
PnR SETTINGS

- Tight correlation is needed as timing vary between corners
- This is even more challenging due to low voltage effects
- Timing fixes increase power consumption and TAT
- Signoff settings applied along PnR stages:
  - POCV Analysis using CCS libraries
  - Enabled extended moments and constraint variation
  - Added additional σ for hold constraint variation
- Power signoff tool invoked along the PnR flow to perform time-based analysis and generate a refreshed GL SAIF for the PnR tool (uses RTL fsdb as an input)

PnR SETTINGS

- Timing convergence comparison - implementation against signoff:





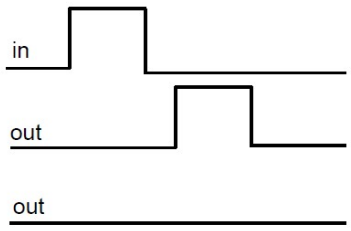
POWER ESTIMATION

- Due to the nature of the design, glitch power has significant contribution to total (GL time-based) power estimation
- Logic simulation is performed with either inertial or transport delays:
  - inertial delays (default)- pulses whose widths are less than the cell delay are absorbed
  - transport delays- pulses narrower than the cell delay propagate to the output

input_pulse < cell delay

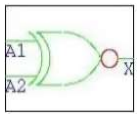
Transport Mode

Inertial Mode

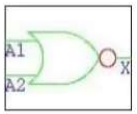


POWER ESTIMATION

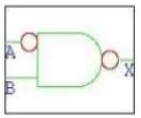
- Logic simulation settings define thresholds for pulse rejection and X transition interpretation
- For proper power analysis, it is recommended to use the most restrictive settings. i.e, reject only pulses which are less than 0% of the cell path delay and generate no Xs (as they are not considered as glitch transitions by the tool)
- Aiming for correct yet more permissive settings, we were looking for a proper glitch filter
- Analyzing the library cells prevalence, we identified 3 glitchy candidates:



EN2_CAQV2



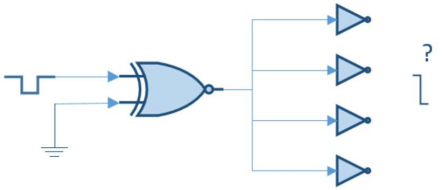
NR2

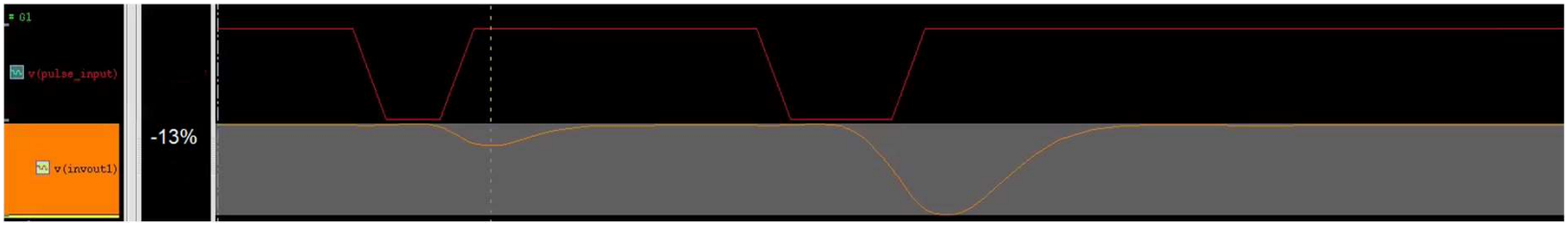


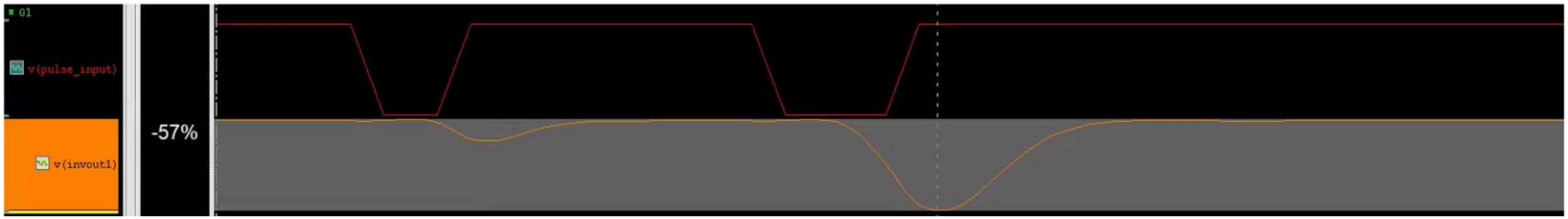
ND2B

POWER ESTIMATION

- We then simulated the largest glitch that these cells filter away:







POWER ESTIMATION

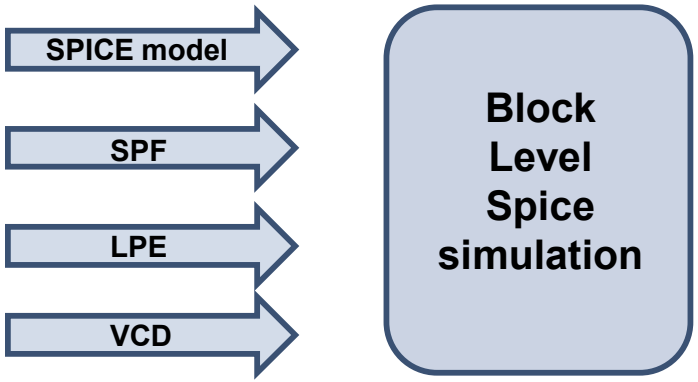
- Taking the minimal pulse width (out of the 3 simulated cells) and dividing it by the largest cell delay, we got 70% glitch filter

- This filter was used by the logic simulator to generate gate level VCD

- Total power was lower than the initial result (0% filter), but still much higher than zero-delay simulation

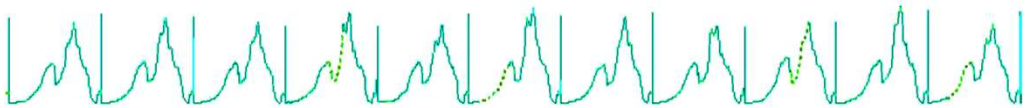
POWER ESTIMATION

- Starting with early power analysis, via glitch analysis in cell level, we took another step forward to estimate power in hierarchy level:
  - Small representative sub-block (RTL -> netlist)
  - Separate logic simulation (VCD)
  - RC extraction using stdcell cdl (SPF)

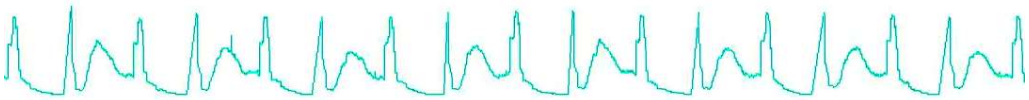


POWER ESTIMATION

- Realistic simulation for custom cells evaluation
- Waveform and spike validation:
  - Spice AVG measurement of total power along specific timing window



  - Power signoff tool waveform

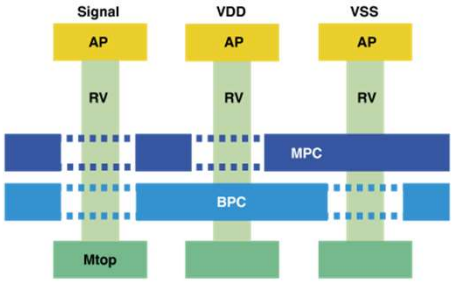


- Total power estimations strongly correlate

POWER GRID ROBUSTNESS

- As nominal voltage goes lower, IR drop becomes more concerning
- The IR drop budget of ~2% here is extremely low absolute value (a few millivolts)

- MIM capacitor insertion significantly improved grid capacitance, reducing IR drop



SILICON PROVEN METHDOLOGY

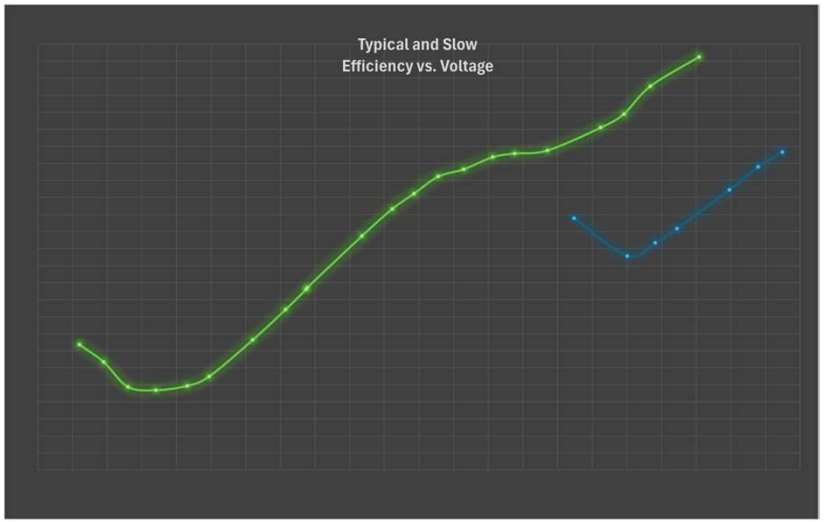
- Post-Si measurements: IR drop ≤ 2%
- IR drop inside the die is relatively low:

Layer Based Drop

Layer	**Max Drop** (%)
RDL *(including package)*	75%
M0-Mtop	25%

SILICON PROVEN METHDOLOGY

- Post-Si leakage (avg) measurements and simulated leakage power are as close as 3%
- Post-Si dynamic power measurements and simulated dynamic power are as close as 1%
- Proper function (verified by logic bist) at nominal voltage and target frequency was achieved:



SUMMARY

- Cutting edge technology provided benefit and challenges
- Low operating voltage achieved by library re-characterization
- Early exploration reduced TAT
- Strong PnR flow allowed smooth convergence
- Glitch filter techniques applied
- Reliable power estimation
- Robust power grid
- Silicon proven methodology

THANK YOU!

ELECTRICAL EFFICIENCY IN CRYPTO MINING

Given by the amount of hashes to generate 1 BTC, the energy it consumes and its cost:

$$\frac{TH}{BTC} X \frac{J}{TH} X \frac{\$}{J} = \frac{\cancel{TH}}{BTC} X \frac{\cancel{kWh}}{\cancel{TH}} X \frac{\$}{\cancel{kWh}} = \frac{\$}{BTC}$$

$$\gg \quad \frac{\$}{BTC} \sim \frac{J}{TH}$$

CELL DELAY AT SLOW CORNER

Cell delay at LT slow corner is 10x higher than HT fast:

LVT INV CCS SS LT

```
timing () {
        related_pin : "A";
        timing_sense : negative_unate;
        timing_type : combinational;
        cell_fall (tmg_ntin_oload_8x7) {
                index_1 ("0.01431, 0.03283006, 0.07531884, 0.1727967, 0.396431, 0.9094932, 2.086562, 4.787");
                index_2 ("2.2235e-05, 7.51161e-05, 0.0002537634, 0.0008572842, 0.002896148, 0.009784004, 0.03305312");
                values ("0.02747132, 0.03019[illegible]836, 0.1598533, 0.4719751, 1.530805", \
                "0.03779422, 0.04100043, 0.[illegible]07042, 0.4861879, 1.54443", \
                "0.05763849, 0.06168231, 0.[illegible]26, 0.5199101, 1.5781", \
                "0.09645565, 0.1025247, 0.[illegible]0.594084, 1.654098", \
                "0.1571921, 0.169417, 0.2[illegible].7554898, 1.823354", \
                "0.2419427, 0.2653128, 0.3[illegible]1.066873, 2.211853", \
                "0.3437519, 0.3856576, 0.45[illegible]1.652793, 2.990072", \
                "0.4450419, 0.5132327, 0.702[illegible], 2.813505, 4.448864");
        }
        wave_fall (1, 2);
        cell_rise (tmg_ntin_oload_8x7) {
                index_1 ("0.01431, 0.03283006, 0.07531884, 0.1727967, 0.396431, 0.9094932, 2.086562, 4.787");
                index_2 ("2.2235e-05, 7.51161e-05, 0.0002537634, 0.0008572842, 0.002896148, 0.009784004, 0.03305312");
                values ("0.03317178, 0.03672277, 0.04804695, 0.08487159, 0.2078051, 0.6212896, 2.023553", \
                "0.04434367, 0.04845621, 0.06102611, 0.09911913, 0.222369, 0.6379534, 2.034575", \
                "0.06561866, 0.07061747, 0.08596734, 0.1294151, 0.2559017, 0.6725046, 2.071774", \
                "0.1080984, 0.114271, 0.1327695, 0.1855459, 0.3273598, 0.747635, 2.1493", \
                "0.1795196, 0.1925924, 0.2255235, 0.293292, 0.4651561, 0.9207625, 2.325851", \
                "0.2849895, 0.3100706, 0.3743003, 0.5030824, 0.7233683, 1.263584, 2.733561", \
                "0.4303154, 0.4743155, 0.5928558, 0.8394879, 1.233273, 1.901407, 3.584702", \
                "0.6281136, 0.6996359, 0.8963867, 1.337174, 2.091239, 3.145993, 5.189567");
        }
```

LVT INV CCS FF HT

```
timing () {
        related_pin : "A";
        timing_sense : negative_unate;
        timing_type : combinational;
        cell_fall (tmg_ntin_oload_8x7) {
                index_1 ("0.004412, 0.008626806, 0.01686804, 0.03298216, 0.06449018, 0.126098, 0.24656, 0.4821");
                index_2 ("2.4805e-05, 8.907172e-05, 0.0003198456, 0.001148527, 0.004124218, 0.01480956, 0.05317933");
                values ("0.003957536, 0.004372631[illegible]909488532, 0.02192324, 0.06611174, 0.224345", \
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        }
        wave_fall (1, 2);
        cell_rise (tmg_ntin_oload_8x7) {
                index_1 ("0.004412, 0.008626806, 0.01686804, 0.03298216, 0.06449018, 0.126098, 0.24656, 0.4821");
                index_2 ("2.4805e-05, 8.907172e-05, 0.0003198456, 0.001148527, 0.004124218, 0.01480956, 0.05317933");
                values ("0.004338712, 0.004764254, 0.006071197, 0.009853889, 0.02216826, 0.06575962, 0.2222633", \
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                "0.009344658, 0.01045368, 0.01349209, 0.02029687, 0.03563269, 0.08162376, 0.2382275", \
                "0.01191138, 0.01339752, 0.01781207, 0.02796613, 0.04733362, 0.09736305, 0.2560434", \
                "0.01518518, 0.01725715, 0.02326927, 0.03798232, 0.06694815, 0.1239425, 0.2903989", \
                "0.01940127, 0.02211571, 0.03025935, 0.05068392, 0.0931649, 0.1685208, 0.3499517", \
                "0.02517096, 0.02860283, 0.03929261, 0.06699572, 0.1271797, 0.2396115, 0.4494317");
        }
```