Chiplet & Advanced packaging The Future of Semiconductor Integration

ChipEx2025

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HELLO!

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AGENDA

- Introduction
- What is Chiplet
- Advanced Packaging types and applications
- 3DBlox as standardization Flow
- Die-to-Die Interfaces
- Standard and Custom UCIe
- Summary

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WHO WE ARE

Avnet ASIC Israel

- Your partner for ASIC design & Turnkey manufacturing
- Offering flexible solutions & business models
- Full range of ASIC services (down to 3nm EUV, 2nm WIP) from specification to mass production, with robust design practices & smooth ramp-up to mass production
- In-house RISC-V CPU family and HW security modules
- Strong in-house productization capabilities (testers, handler)
- TSMC VCA Partner – silicon channel for customers

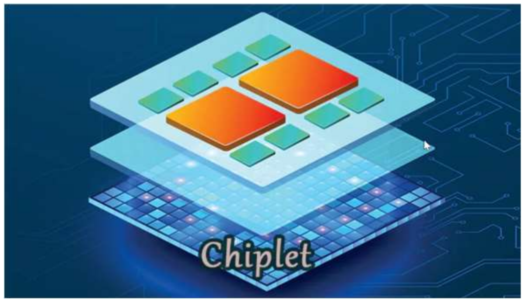
All services under one roof

35 years of experience

Hundreds of successfully completed projects

What is Chiplet in Advanced Packaging?

A **Chiplet** is a **modular integrated circuit (IC)** designed to perform a specific function and work together with other Chiplets inside a single chip package



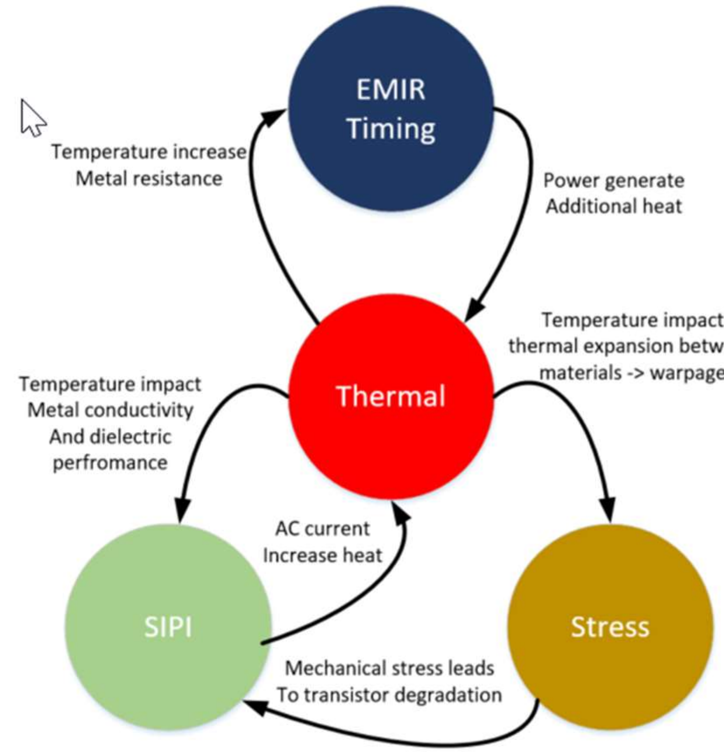
Era / Concept	*Description*
MCM (Multi-Chip Module)	*Emerged in the 1980s–90s: multiple **bare dies** placed on a substrate to work as a system. Focus was on **integration density** and reducing board area.*
SiP (System-in-Package)	*Broader and more flexible than MCM — integrates **heterogeneous dies** (logic, memory, analog, RF, sensors) in one package.*
Chiplet Architecture	*Takes SiP further by using **standardized, modular dies** that are **designed to interoperate** — not just be co-packaged. Chiplets are a **design methodology**, not just a packaging technique.*

Why Chiplets?

Benefit	*Explanation*
Improved yield	*Smaller chips have fewer defects, improving wafer yield and reducing cost.*
Heterogeneous integration	*Combine logic, memory, analog, I/O, or accelerators built on different process nodes.*
Design reuse	*The same chiplet can be reused across multiple products or platforms.*
Faster time-to-market	*Teams can work on different chiplets in parallel and integrate them later.*
Scalability	*Enables modular upgrades (e.g., scale CPU/GPU/AI cores or memory bandwidth).*

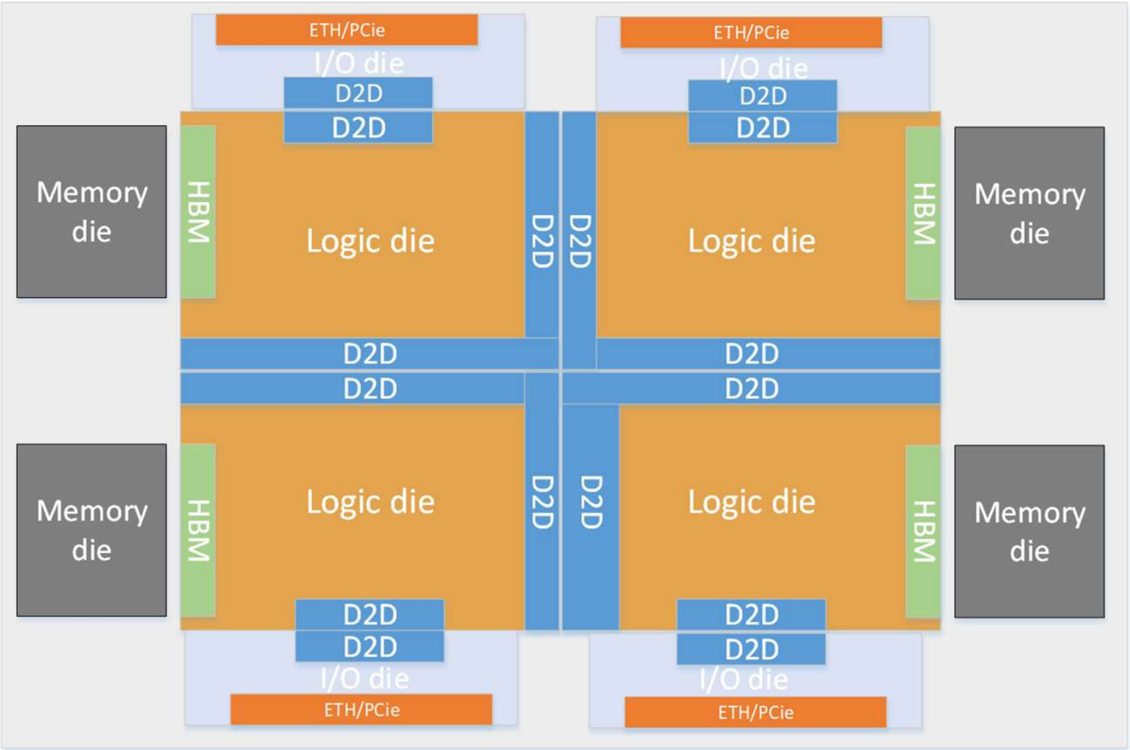
Advanced Packaging Challenges

Challenge	Cause / Root
Package Warpage	Large interposer or organic substrate area with many dies
Die Shift / Misalignment	Uneven thermal expansion (CTE mismatch), bonding pressure
Stacked Die Hotspots	3D stacking or dense die proximity (logic + memory + accelerator)
Inadequate Heat Dissipation	Lack of direct contact to heat sink (middle layers in 3D)
IR Drop / PDN Collapse	Shared PDN across Chiplets, long redistribution paths, TSV resistance
Uneven Power Delivery	Different Chiplet power profiles, asymmetric loading
Lossy Die-to-Die Interfaces	Long traces, interposer metal losses, dielectric properties
Crosstalk / Skew	Dense bump patterns, insufficient shielding, variation in trace impedance



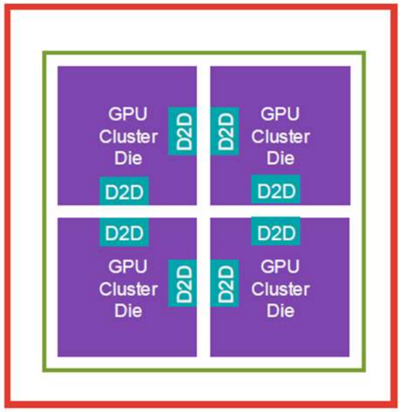
Advanced packaging Application Types

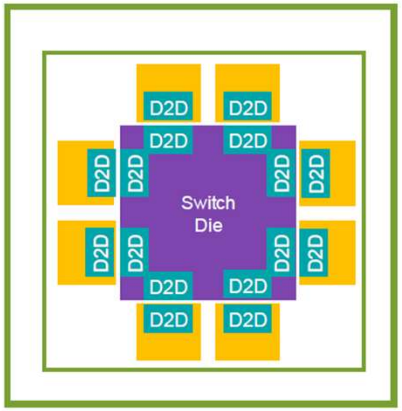
- Logic die – can be CPU/GPU/AI
  Can be done as 3D stacking
- IO die – purpose to connect between
  External and internal interfaces
- Memory – HBM2/2E/3/3E and CHBM
  all are done with 3D stacking
- D2D interface is for :
  - Standard package
  - Advanced package
  - 3D stacking

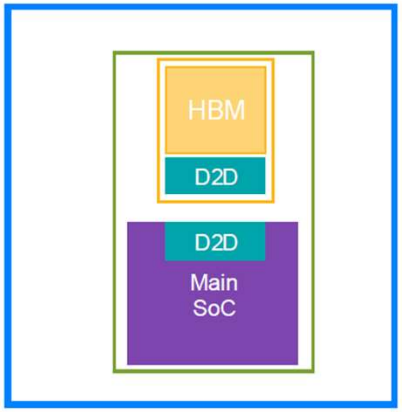


Applications that benefit from High Bandwidth Die-to-Die

Very Large AI Training SoCs	100T Switch SoC Optical & Electrical	Custom HBM Base Die	High BW D2D over Substrate
Area & power efficiency	Edge occupancy	Edge BW efficiency	Package cost reduction







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Advanced Packaging Standartization

- 3Dblox is 3D Chiplet design data exchange format that enables 2.5D/3D dies integrations
- Unify physical, logical and connectivity information for EDA and supply chains
- Enables multi-vendor interoperability ,simplifies top-down planning
- Chiplet placement and floorplaning, system planning , verification across dies
- Supported by major EDA vendors : Synopsys, Cadence, Siemens, Ansys
- Adopted by UCIe, OCP ODSA, and Intel, AMD, TSMC, Samsung, DARPA CHIPS

3Dblox Physical Flow

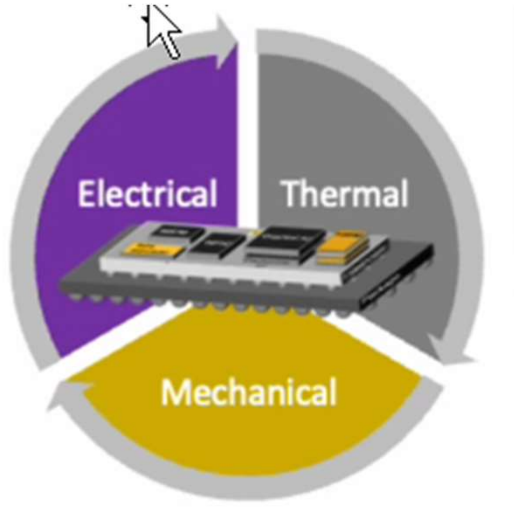
Feasibility
- PDN Feasibility
- Thermal Feasibility

➢ Early Design exploration on 3D Floorplans

➢ Taking in Account Power, Thermal, Mechanical budget

Prototyping
- Floorplan-driven Tile-based Bump Synthesis
- Routability-driven Bump Assignment

➢ Resource Planning on Chiplet Interfaces



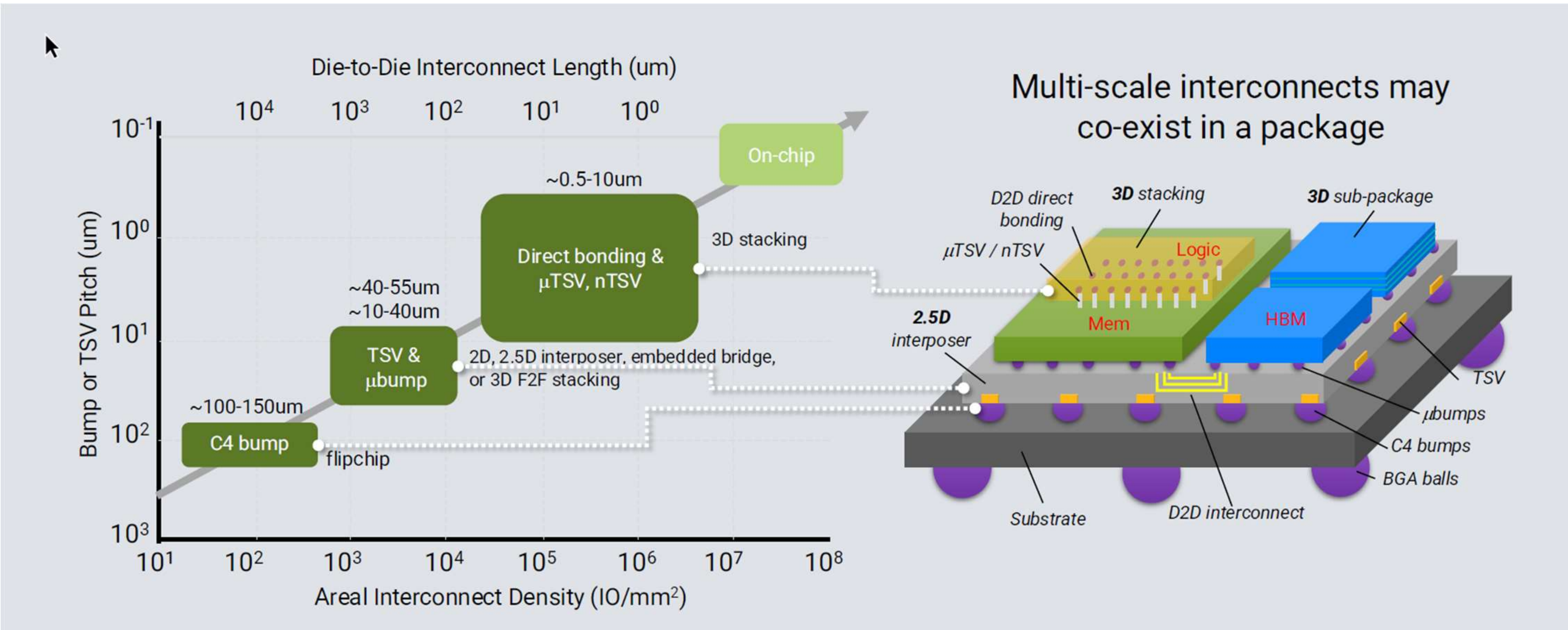
Implementation
- Chiplet Mirroring
- Testing Extension
- Inter-chiplet DRC

➢ Chiplet Design Reuse

➢ Test Planning

➢ Integrated 3D System DRC

Advanced Packaging interconnect structure



Source: Xi-Wei Lin et al., IEDM 2021

Advanced Packaging Interconnect Types

Parameter	Silicon Interposer (2.5D)	RDL Organic Interposer	Hybrid Interposer (Si + RDL)	Laminate Substrate	3D Stacking (Hybrid Bonding)
Bump Pitch (µm)	40–65	40–65	40–65	90–150	1.6–9
I/O Density (IO/mm²)	High (500–1000)	High (500–1000)	High (500–1000)	Low (50–200)	Ultra High (>10,000)
Trace Width/Spacing (µm)	0.4–2 / 0.4–2	2–6 / 2–6	2–6 / 2–6	8–20 / 8–20	0.5–2 / 0.5–2
Energy per Transmit (pJ/bit)	Low (~0.1–0.5)	Medium (~0.5–1.0)	Medium–Low (~0.3–0.8)	Medium–High (1–3)	Very Low (~0.05–0.2)
Relative Cost	High	Medium	Medium–High	Very Low	Extra High

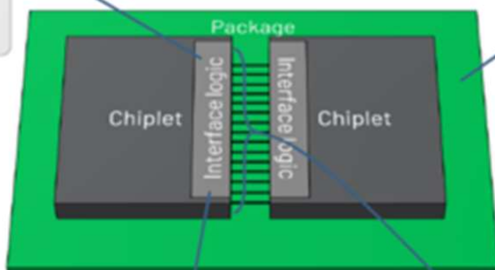
Die-to-Die Interface Selection

Energy Consumption

- Energy is needed to send data across interface
- Efficiency measured in **pJ/bit**
- 1 Tbit/s at 1pJ/bit = 1 W

Packaging Requirements

- Bump pitch drives package cost
  - >110 µm → laminate
  - <110 µm → Fan-Out, silicon bridge, interposer



Latency

- Speed to get data across interface
- Strongly influenced by type of error correction
- Latency measured in **ns** or **clock cycles**

Bandwidth Density

- Interface logic and pinout consume area and bumps
- Measured in **Gbps/mm**

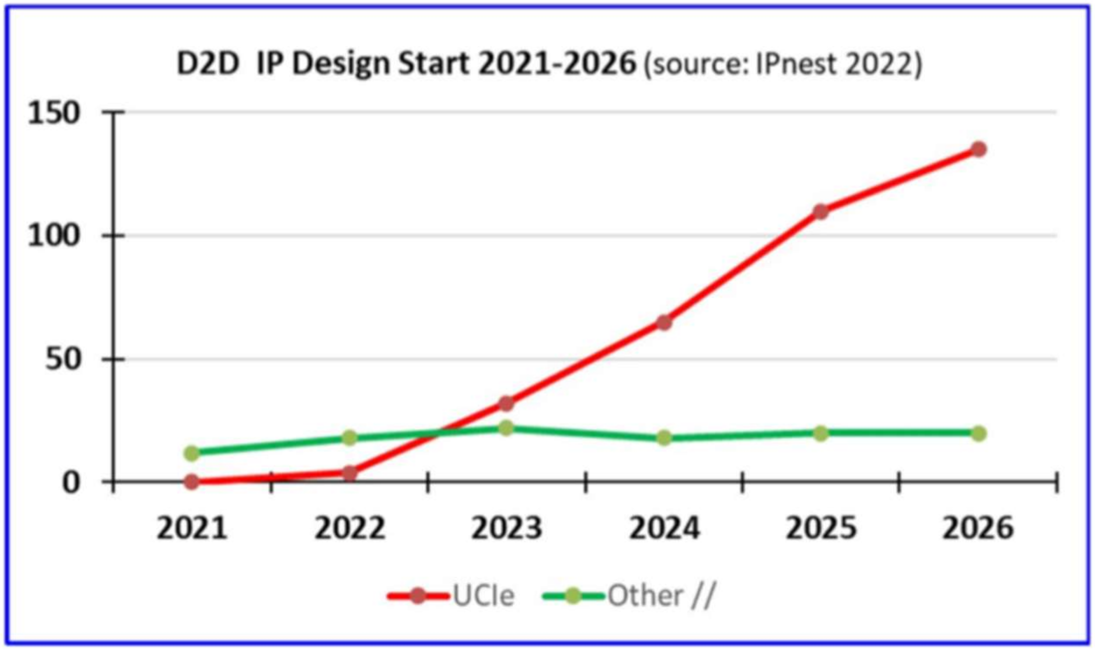
Die-to Die Interfaces Comparison

Die-to-Die Interface	Ultra Short Reach SerDes (XSR/USR)	Bunch of Wires (BoW)	Advanced Interface Bus (AIB)	Universal Chiplet Interface (UCIe)	Photonic
Adoption	Industry standard / in production	~ 10 companies designing with BoW	~ 10x 3rd party chiplets, Intel's chiplets	~120 member companies	Active R&D phase, challenges in packaging, energy
Package	laminates	standard, advanced	advanced packaging	standard, advanced	Requires photonic I/Os, silicon interposers
Bump Pitch	130-170 µm	45-170 µm	25 - 55 µm	10-130 µm	N/A (uses photonic I/Os)
Lane Rate	112 G / 224 G	2 - 32 Gbps	2 - 6.4 Gbps	4 - 32 Gbps	Multiple wavelengths each at 25-50Gbps
Latency	~10 ns	< 2 ns	< 2 ns	< 2 ns	Comparable or lower than electrical with advanced packaging
Reach	< 50 mm	< 25 mm	< 25 mm	< 10 mm	Dependent on optical link length, can exceed meters on chip
Bit Error Rate	<1E-15, <1E-6 w/ FFC	<1E-15	n/a	<1E-15 to <1E-27	Forward error correction targets below 10^-15
Energy	1-4 pJ/bit	0.3-0.5 pJ/bit	0.5-0.8 pJ/bit	0.25-0.5 pJ/bit	0.1-1pJ/bit depending on link length and technology
Edge Density	< 3 Tbps/mm	< 4 Tbps/mm	< 1.6 Tbps/mm	< 10 Tbps/mm	Multiple Tb/s per mm^2 achievable with dense WDM
Link Layer	Not Defined	BoW link layer, supporting AXI, CHI	AXI	Raw, Streaming, PCIe, CXL	Physical layer handles modulation/detection of light
Target Applications	Optical Networking	Disaggregation, e.g AI accelerators, automotive	Aerospace & defense ecosystem	Scale & split, system aggregation	High-performance computing, data centers, AI acceleration

Die-to-Die Interfaces Comparison

Interfaces	Strengths	Challenges
XSR./USR	High bandwidth: Offers good data rates with reasonable complexity. Scalability: Can support multiple lanes for increased bandwidth. Established technology: Mature technology with readily available IP blocks.	Power consumption: Higher power consumption compared to BoW or UCIe. Complexity: Requires SerDes expertise for design and implementation. Latency: Serialization adds latency compared to parallel interfaces.
BoW	Low power: Very low power consumption due to simple parallel design. Simple design: Relatively easier to design and integrate. Open standard: Fully open-source, promoting customization and flexibility.	Limited bandwidth: Lower data rates compared to SerDes or UCIe. Scalability: May face challenges scaling to larger chiplet configurations. Adoption: Not as many industry adoption compared to UCIe.
AIB	High bandwidth: Supports very high data rates for demanding applications. Flexibility: Offers various protocol options depending on the vendor. Established technology: Backed by large companies like Intel.	Complexity: Highly complex design, requiring additional development effort. Potentially high cost: May be more expensive due to proprietary technology. Limited interoperability: Might not be compatible with other chiplet solutions.
UCIe	Broad industry support: Backed by major players, ensuring wider adoption and interoperability. Flexibility: Supports various protocols like PCIe, CXL, and Gen-Z for diverse applications. Scalability: Designed for future scaling with higher bandwidth and denser integration.	Complexity: Multiple options can lead to longer design times and higher complexity. Potentially vendor lock-in: While open, some aspects are still controlled by individual vendors. Limited silicon availability: Not all foundries offer UCIe-compliant packages yet.
Photonic	Ultra-high bandwidth: Offers potentially limitless bandwidth for future needs. Low power consumption: Can be more power-efficient than electrical interconnects. Reduced crosstalk: No electrical interference between signals.	Immature technology: Still in early stages of development, with many challenges to overcome. High cost: Currently very expensive due to limited adoption and complex manufacturing. Integration challenges: Requires specialized packaging and design expertise.

Dominant Die-to-Die is UCIe



D2D Design Start IP Forecast 2021-2026

芯耀辉 | AkroStar, Alibaba Group, alchip, Amkor Technology, ANALOG DEVICES
apmemory, AsteraLabs, 芯云凌 Atrontech, AVERY design systems
AyarLabs, blaize, BLUE CHEETAH ANALOG DESIGN, BROADCOM
BlueOcean Smart, Brite semiconductor, cadence, CXMT 长鑫存储技术有限公司
DECA, Octopus, GUC The Advanced ASIC Leader, InPsytech
INNOSILICON, JCET, kiwi moore
KNIULINK, M² SEMI 超摩科技
MEDIATEK, Micron, MICROCHIP, 摩尔精英 MooreElite.com
nepes corporation, NEURON IP, openfive, oppo
proteanTecs, SOFICS, SmartDV, SPIL 矽品精密 Siliconware
希姆计算 STREAM COMPUTING, SYNOPSYS Silicon to Software, Tachyum, Universal Instruments
WILDER TECHNOLOGIES, VeriSilicon, XPEEDIC

UCIE Main Parameters

Feature	UCIe parameter
Data Rate	16–32 Gbps per lane (current), future plans 64 Gbps and beyond
Latency	Ultra-low (sub-nanosecond range)
Power Efficiency	High (supports adaptive voltage scaling)
Lane Width	Flexible (typical widths: x16, x32, x64, x128 lanes)
Physical Interface	Supports both parallel (advanced packaging) and serial interfaces
Supported Protocols	PCIe, CXL, CCIX, proprietary
Packaging Types	Organic substrate, 2.5D, 3D stacking

UCIE KPI For Different Interconnect types

Characteristics / KPIs	*UCIe-S (2D)*	*UCIe-A (2.5D)*	*UCIe 3D*
Data Rate (GT/s)	*4, 8, 12, 16, 24, 32*		*Up to 4*
Width (each cluster)	*16*	*64*	*80*
Bump Pitch (µm)	*100 – 130*	*25 – 55*	*1.6-9*
Channel Reach (mm)	*≤ 25*	*≤ 2*	*3D vertical (FtF bonding initially; FtB, BtB, multi-stack possible)*
BW Density (GB/s/mm²)	*22 – 125*	*188 – 1350*	*4,000 – 300,000 (4TB/s/mm² @9µm, ~12TB/s/mm² @5µm, ~35TB/s/mm² @3µm, ~300TB/s/mm² @1µm)*
Power Efficiency Target (pJ/b)	*0.5*	*0.25*	*<0.05 at 9µm → 0.01 at 1µm*
Latency	*< 2ns*	*<0.5 ns*	*<0.1ns*

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Future Trends For Custom UCIe

- Standard substrate has a bigger bump pitch signal width/space than 2.5 Interposer
- Currently in development better metrics for standard substrate

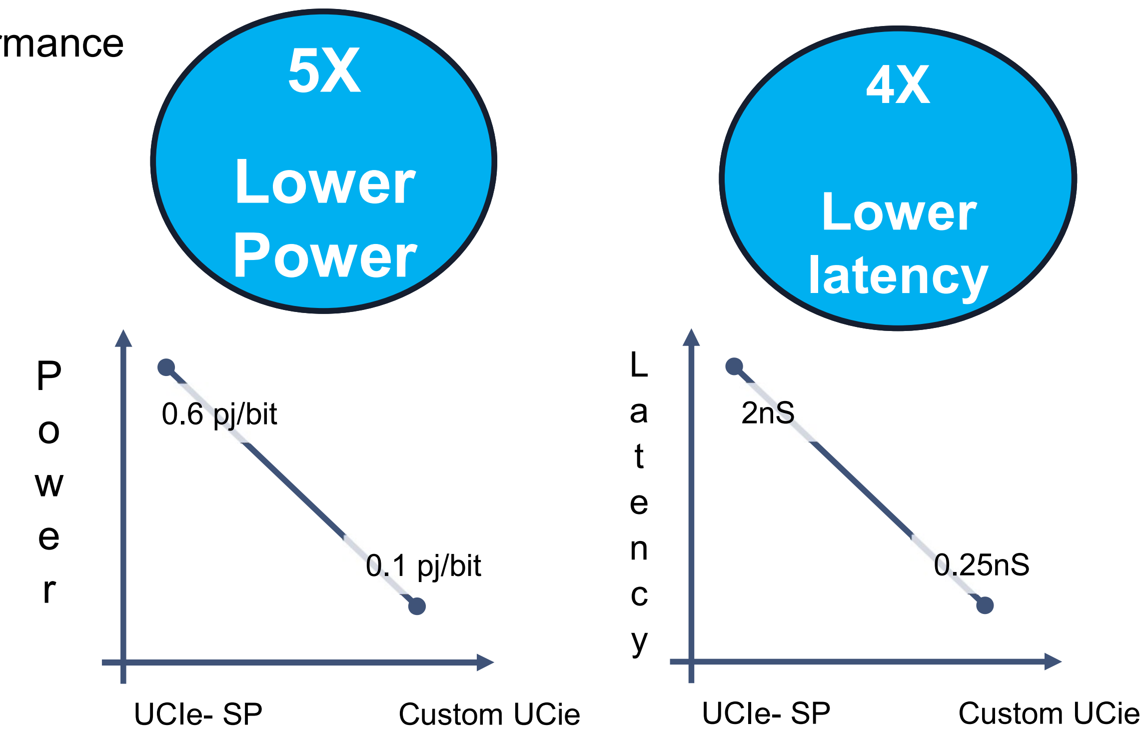
Metric	***Today (standard ABF)***	***In development***
Bump pitch	*100–130 µm*	*40–60 µm*
Line/space (L/S)	*5–8 µm*	*2–3 µm*

- Better bump and signal pitch will bring high IO density, better bandwidth/mm and low power per bit
- In addition, custom UCIE may allow flex bumps to optimize die area

Future Trends for Custom UCIe

- Standard substrate can provide similar Performance

For D2D communication as 2.5D Interposer



Key Take Aways

- **Growth Drivers**: Design reuse, yield, time-to-market, scalability
- **Standardization**: 3dBlox enables common chiplet flow
- **Key KPIs**: Bandwidth, latency, power, cost
- **Interface**: UCIe = leading D2D standard
- **Packaging**: 2.5D for performance, standard for cost

THANK YOU!