Power Efficient Implementation Flow

with *Synopsys* tools and *SiliconSmart* Characterization

Ron Blum | ASIC Project Lead

Avnet ASIC Israel

Agenda

Agenda

- Introduction
- Technology adaptation and challenges
- Re-Characterization
- STA
- RTLA early exploration
- PnR flow
- Power estimation
- Power grid
- Post-Si measurements

Introduction

Avnet ASIC Israel

- Your partner for ASIC design & Turnkey manufacturing
- Offering flexible solutions & business models
- Full range of ASIC services (down to 4nm EUV, 3nm WIP) from specification to mass production, with robust design practices & smooth ramp-up to mass production
- In-house RISC-V CPU family and HW security modules
- Strong in-house productization capabilities (testers, handler)
- TSMC VCA Partner – silicon channel for customers

All services under one roof

35 years of experience

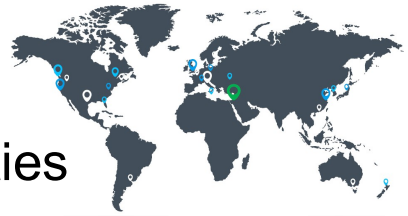
Hundreds of successfully completed projects

Blockstream Israel

- Blockstream is a leading provider of blockchain technologies and remains on the forefront of work in cryptography and distributed systems
- Blockstream Israel, the corporate ASIC division, is a trailblazer in the Bitcoin arena, aiming to accelerate Bitcoin mining capabilities
- We are in a mission to launch the world's first enterprise-class miner
- Leveraging the unparalleled security of Bitcoin, we construct crypto-financial frameworks aimed at enhancing market efficiency and reducing reliance on trust

Blockstream

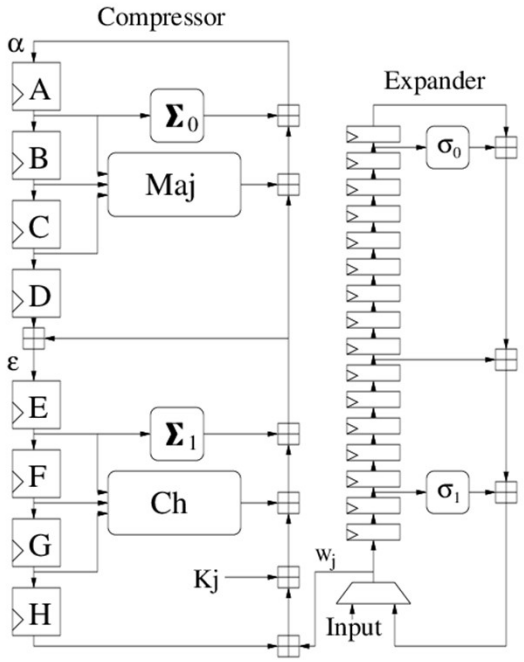
Assaf Gilboa
EVP of Hardware Engineering
Founder of Spondoolies, expert in ASIC design, embedded systems, and networking.



Crypto Mining Application

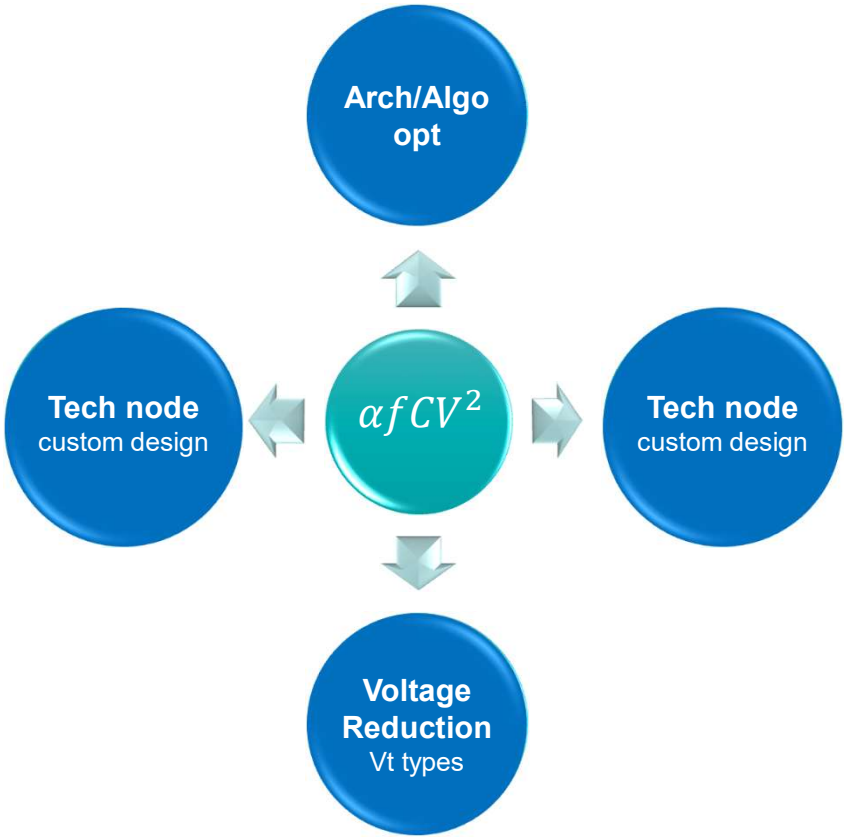
Properties

- Implementation of DSHA-256 hashing algorithm
- Pure Stdcell
- Extensive performance
- Arithmetic logic susceptible to glitches
- Substantial dynamic power



Crypto Mining Application

Dynamic Power Reduction

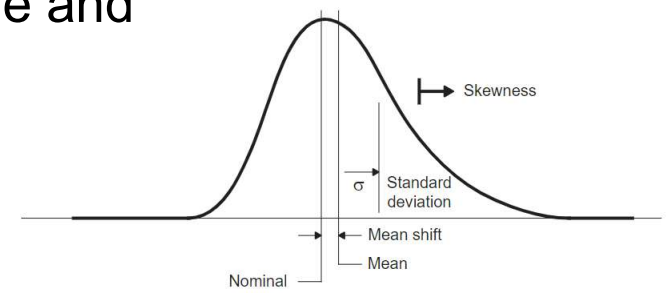


Technology
adaptation and challenges

Technology

Advanced node facilitates power reduction

- TSMC advanced node improves both density and power
- Ultra-Low Vt and Extreme-Low Vt cell types selected
- Significantly slow transistors at low temperature
- Special signoff conditions: extended hold constraint (μ+3σ), moment-based asymmetric delay distribution, voltage and temperature margin, wire ocv, spatial ocv



Technology

Advanced node facilitates power reduction

- Additional placement limitations


```
Information: VT group G1_N found
Information: Layers VTEL_N(1202) VTL_N(12) VTS_N(23) are added to VT group G1_N
Information: Setting VT group G1_N min width to 0.153
Information: VT group G2_N found
Information: Layers VTUL_N(151) VTLN_LL(1204) are added to VT group G2_N
Information: Setting VT group G2_N min width to 0.153
Information: VT group G3_N found
Information: Layers VTULN_LL(1515) VTL_N(12) VTLN_LL(1204) are added to VT group G3_N
Information: Setting VT group G3_N min width to 0.153
Information: VT group G4_N found
Information: Layers VTEL_N(1202) VTUL_N(151) are added to VT group G4_N
Information: Setting VT group G4_N min width to 0.153
Constructing VT legality info...
```

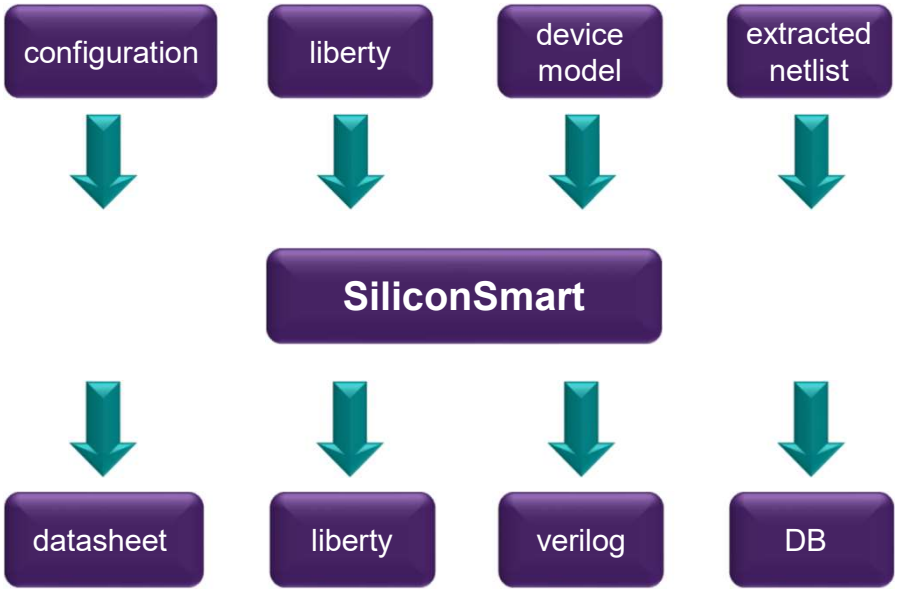
Re-Characterization

SiliconSmart

Re-Characterization

Lower operating voltage facilitates power reduction

- Further optimization by re-characterization of TSMC libraries for low voltage $(< \frac{std\ Volt.}{2} \pm 10\%)$ within application typical temperature range



STA
PrimeTime

STA

Low voltage signoff conditions

- Special flow is required near threshold when $V_t + 50mV \leq VDD \leq V_t + 125mV$:
  - additional σ for hold constraint variation (i.e, μ+**4**σ)

```
set_app_var timing_pocvm_corner_sigma 3
set_app_var timing_pocvm_report_sigma 3
```

Linear Sum
P (μ+4σ,0)

```
set search_path <CCS LVF path>
set_timing_derate -cell_check \
-pocvm_coefficient_scale_factor 0 -early
set_timing_derate -cell_check \
-pocvm_subtract_sigma_factor_from_nominal \
-4 -early
```

```
set search_path <CCS MARGIN LVF path>
set_timing_derate -cell_check \
-pocvm_coefficient_scale_factor 0 -early
set_timing_derate -cell_check \
-pocvm_subtract_sigma_factor_from_nominal \
-1 -early
```

RSS
P (μ+σ,3σ)

```
set search_path <CCS LVF path>
set_timing_derate -cell_check \
-pocvm_subtract_sigma_factor_from_nominal \
-1 -early
```

```
set search_path <CCS MARGIN LVF path>
set_timing_derate -cell_check \
-pocvm_subtract_sigma_factor_from_nominal \
2 -early
```

STA

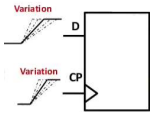
Low voltage signoff conditions

```
set timing_pocvm_enable_extended_moments true
set timing_pocvm_enhanced_moment_near_vth_voltage true
```

-wider range for transition variation:

data transition: μ+2σ

clock transition: μ+3σ




```
set timing_pocvm_max_transition_sigma 2
set timing_pocvm_max_transition_clock_sigma 3
```

- CRPR sigma removal is disabled in min-pulse-width check

```
set timing_crpr_different_transition_variation_derate 0.0
```

- considering input transition variation impact on constraint variation

```
set_app_var timing_enable_constraint_variation true
set timing_use_slew_variation_in_constraint_arcs setup_hold
```

STA

Low voltage signoff conditions

- slow corner delays are 10x higher than fast:

LVT INV CCS SS LT

```
timing () {
        related_pin : "A";
        timing_sense : negative_unate;
        timing_type : combinational;
        cell_fall (tmg_ntin_oload_8x7) {
                index_1 ("0.01431, 0.03283006, 0.07531884, 0.1727967, 0.396431, 0.9094932, 2.086562, 4.787");
                index_2 ("2.2235e-05, 7.51161e-05, 0.0002537634, 0.0008572842, 0.002896148, 0.009784004, 0.03305312");
                values ("0.02747132, 0.0301925, 0.03883802, 0.06664936, 0.1598533, 0.4719751, 1.530805", \
                "0.03779422, 0.04100043, 0.05093523, 0.07[illegible]598, 0.1737042, 0.4861879, 1.54443", \
                "0.05763849, 0.06168231, 0.07[illegible]0.1594331[illegible]2058326, 0.5199101, 1.5781", \
                "0.09645565, 0.1025247, 0.11[illegible]0.2611199,[illegible]18468, 0.594084, 1.654098", \
                "0.1571921, 0.169417, 0.2001[illegible]0.4459908[illegible]53, 0.7554898, 1.823354", \
                "0.2419427, 0.2653128, 0.325[illegible]6593, 1.066873, 2.211853", \
                "0.3437519, 0.3856576, 0.4975[illegible]97643, 1.652793, 2.990072", \
                "0.4450419, 0.5132327, 0.7021309, 1.[illegible], 1.824921, 2.813505, 4.448864");
        }
        wave_fall (1, 2);
        cell_rise (tmg_ntin_oload_8x7) {
                index_1 ("0.01431, 0.03283006, 0.07531884, 0.1727967, 0.396431, 0.9094932, 2.086562, 4.787");
                index_2 ("2.2235e-05, 7.51161e-05, 0.0002537634, 0.0008572842, 0.002896148, 0.009784004, 0.03305312");
                values ("0.03317178, 0.03672277, 0.04804695, 0.08487159, 0.2078051, 0.6212896, 2.023553", \
                "0.04434367, 0.04845621, 0.06102611, 0.09911913, 0.222369, 0.6379534, 2.034575", \
                "0.06561866, 0.07061747, 0.08596734, 0.1294151, 0.2559017, 0.6725046, 2.071774", \
                "0.1080984, 0.114271, 0.1327695, 0.1855459, 0.3273598, 0.747635, 2.1493", \
                "0.1795196, 0.1925924, 0.2255235, 0.293292, 0.4651561, 0.9207625, 2.325851", \
                "0.2849895, 0.3100706, 0.3743003, 0.5030824, 0.7233683, 1.263584, 2.733561", \
                "0.4303154, 0.4743155, 0.5928558, 0.8394879, 1.233273, 1.901407, 3.584702", \
                "0.6281136, 0.6996359, 0.8963867, 1.337174, 2.091239, 3.145993, 5.189567");
        }
```

LVT INV CCS FF HT

```
timing () {
        related_pin : "A";
        timing_sense : negative_unate;
        timing_type : combinational;
        cell_fall (tmg_ntin_oload_8x7) {
                index_1 ("0.004412, 0.008626806, 0.01686804, 0.03298216, 0.06449018, 0.126098, 0.24656, 0.4821");
                index_2 ("2.4805e-05, 8.907172e-05, 0.0003198456, 0.001148527, 0.004124218, 0.01480956, 0.05317933");
                values ("0.003957536, 0.004372631, 0.005666353, 0.009488532, 0.02192324, 0.06611174, 0.224345", \
                "0.00517211, 0.00567282, 0.007088078, [illegible], 0.02413226, 0.06839523, 0.2270529", \
                "0.006581822, 0.007335188, 0.0094[illegible]0.0193863[illegible]0.02813252, 0.07279195, 0.2312099", \
                "0.008233481, 0.009341347, 0.012[illegible]03481668, 0.08123584, 0.2396134", \
                "0.009955134, 0.01146458, 0.015[illegible]0.02619613,[illegible]602974, 0.09639575, 0.2568594", \
                "0.01166242, 0.01368887, 0.0198[illegible]84432, 0.1214547, 0.2891986", \
                "0.01271491, 0.01544323, 0.02354[illegible]03444596[illegible]669866, 0.1636708, 0.3461776", \
                "0.01234736, 0.01591818, 0.02635251[illegible]0.1142898, 0.2280416, 0.4405995");
        }
        wave_fall (1, 2);
        cell_rise (tmg_ntin_oload_8x7) {
                index_1 ("0.004412, 0.008626806, 0.01686804, 0.03298216, 0.06449018, 0.126098, 0.24656, 0.4821");
                index_2 ("2.4805e-05, 8.907172e-05, 0.0003198456, 0.001148527, 0.004124218, 0.01480956, 0.05317933");
                values ("0.004338712, 0.004764254, 0.006071197, 0.009853889, 0.02216826, 0.06575962, 0.2222633", \
                "0.005629321, 0.006091429, 0.007527001, 0.01174129, 0.02445969, 0.06821983, 0.2248906", \
                "0.007279577, 0.008026931, 0.01008008, 0.01487929, 0.02863823, 0.07276533, 0.2293958", \
                "0.009344658, 0.01045368, 0.01349209, 0.02029687, 0.03563269, 0.08162376, 0.2382275", \
                "0.01191138, 0.01339752, 0.01781207, 0.02796613, 0.04733362, 0.09736305, 0.2560434", \
                "0.01518518, 0.01725715, 0.02326927, 0.03798232, 0.06694815, 0.1239425, 0.2903989", \
                "0.01940127, 0.02211571, 0.03025935, 0.05068392, 0.0931649, 0.1685208, 0.3499517", \
                "0.02517096, 0.02860283, 0.03929261, 0.06699572, 0.1271797, 0.2396115, 0.4494317");
        }
```

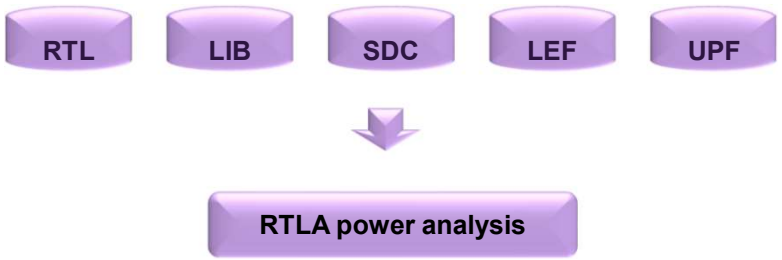
Early RTL Exploration

RTL Architect

Early RTL Exploration

RTLA

- Early RTL exploration facilitated PPA optimization, providing quick feedback before physical implementation flow completes
- RTLA predictive synthesis engine was used to perform reliable power analysis using minimal set of collaterals, enabling short TAT and feedback on custom cells contribution



Early RTL Exploration

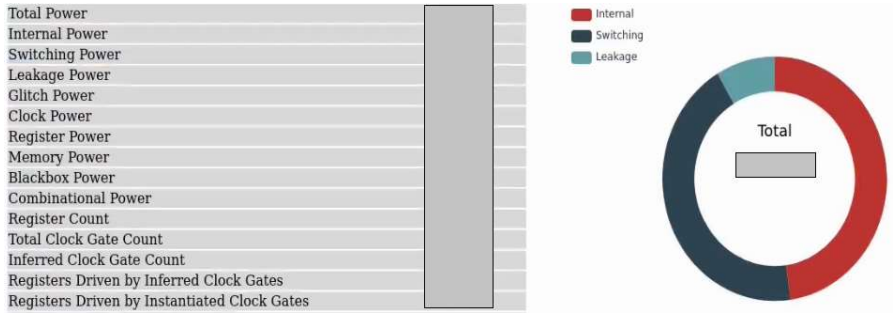
RTLA

- Deviation between RTLA and PrimePower (SDF based GLS):

  Net Switching Power: 0.8%

  Cell Internal Power: 0.4%

  Cell Leakage Power: 16%



- Deviation between RTLA and FC (route stage):

  Cell Count: 4%

  Cell Area: 6%

- Runtime is ~4x faster (initOpto)

PnR Flow
FusionCompiler

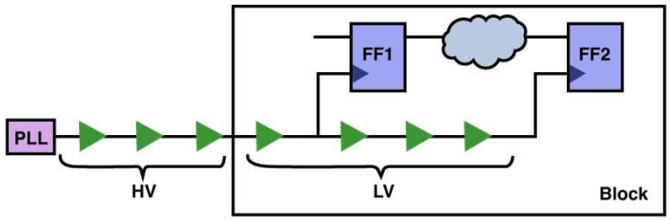
PnR Flow

Clock Tree

- Optimized clock tree, constructed using extreme-low-Vt cells, minimizes the exceptional OCV effects, ensuring low latency
- Clock routing uses triple spacing as needed, serving as a place-holder for incremental fixes (coaxial shielding)

```
create_shields -coaxial_below true
```

- Main clock tree branches are activated in higher voltage, local branches- in low voltage



PnR Flow

Settings

- Tight correlation is needed as timing vary between corners
- This is even more challenging due to low voltage effects
- Timing fixes increase power consumption and TAT
- Signoff settings applied along PnR stages:

  - POCV Analysis using CCS libraries

```
set_app_options -name time.pocvm_enable_analysis -value true
```

  - Enabled extended moments and constraint variation

```
set_app_options -name time.pocvm_enable_extended_moments -value true
set_app_options -name time.enable_constraint_variation -value true
```

PnR Flow

Settings

- Added additional σ for hold constraint variation

```
set_timing_derate -cell_check -pocvm_coefficient_scale_factor 0 -early

set_timing_derate -cell_check -pocvm_subtract_sigma_factor_from_nominal -4 -early
```

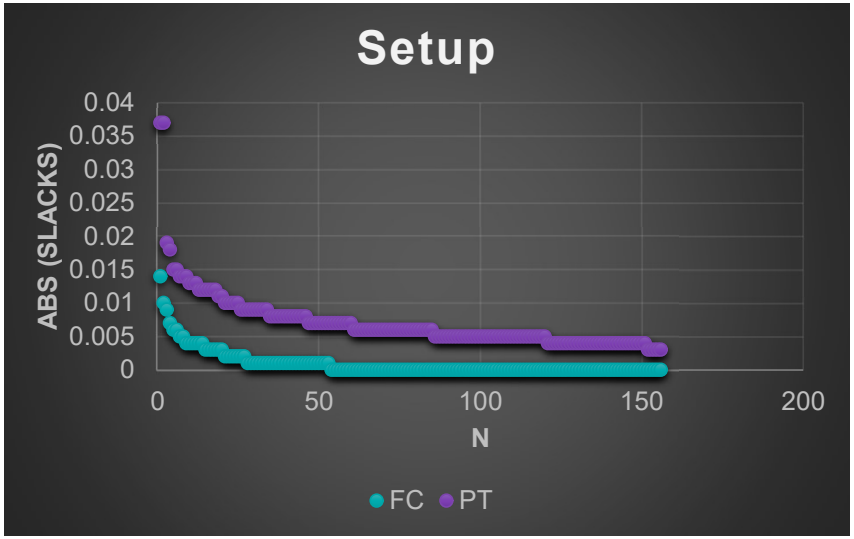
- PrimePower invoked along the PnR flow to perform time-based analysis and generate a refreshed GL SAIF for FC (uses RTL fsdb as an input):

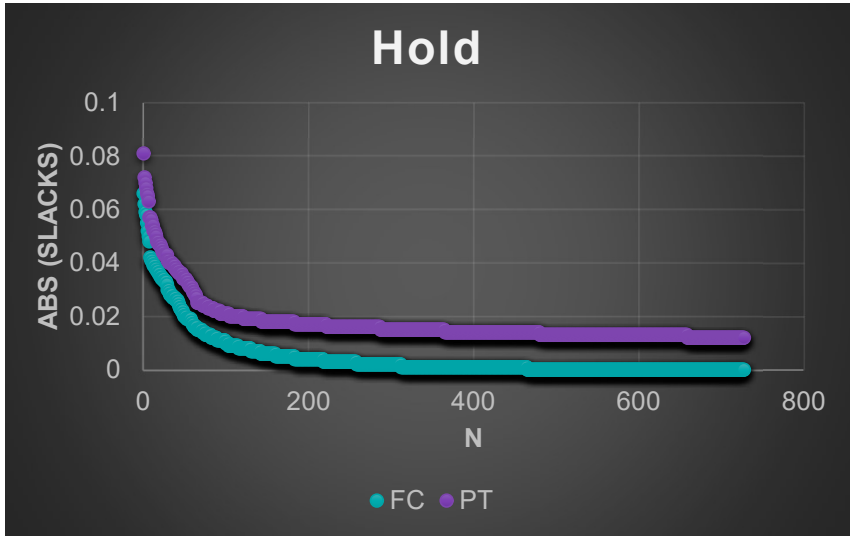
```
set_indesign_primepower_options -fsdbs { { test.fsdb -strip_path "Top/Hier" -format systemverilog \

-analyze_scenarios <power_scenario>} } \

-pwr_shell <pwr_shell path>

-max_cores 16
```

PnR Flow

Timing Correlation

- Timing convergence comparison - FusionComplier against PrimeTime:





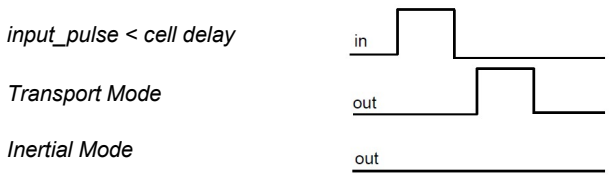
Power Estimation

PrimePower, VCS, PrimeSim, FineSim

Power Estimation

Glitch Filtering

- Due to the nature of the design, glitch power has significant contribution to total (GL time-based) power estimation
- Logic simulation is performed with either inertial or transport delays:
  - inertial delays (default)- pulses whose widths are less than the cell delay are absorbed
  - transport delays- pulses narrower than the cell delay propagate to the output



Power Estimation

Glitch Filtering

- VCS defines thresholds for pulse rejection and X transition interpretation commands
- For proper power analysis, it is recommended to use the most restrictive settings. i.e, reject only pulses which are less than 0% of the cell path delay and generate no Xs (as they may lead to inaccurate estimation)

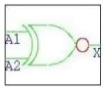
```
+transport_path_delays
+transport_int_delays
+pulse_e/0 +pulse_int_e/0
+pulse_r/0 +pulse_int_r/0
```

- Aiming for correct yet more permissive settings, we were looking for a proper glitch filter

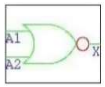
Power Estimation

Glitch Filtering

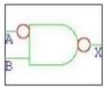
- Analyzing the library cells prevalence, we identified 3 glitchy candidates:



EN2_CAQV2

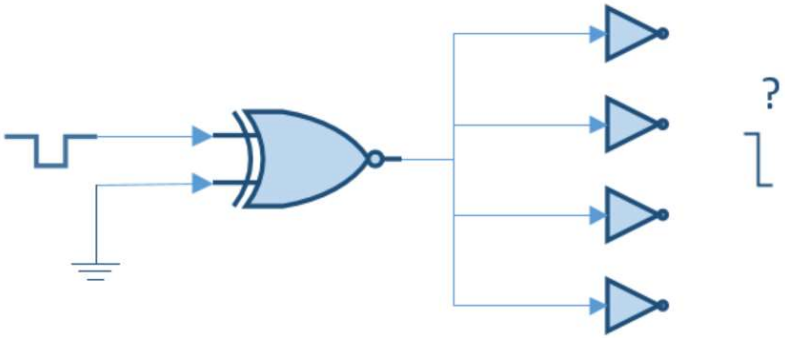


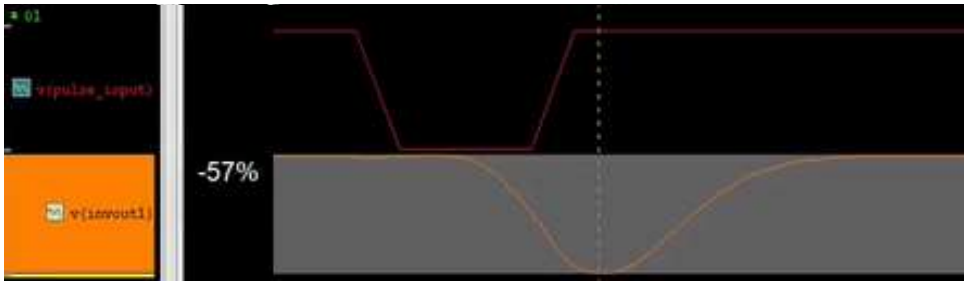
NR2



ND2B

- We then simulated the largest glitch that these cells filter away using *FineSim*:





Power Estimation

Glitch Filtering

- Taking the minimal pulse width (out of the 3 simulated cells) and dividing it by the largest cell delay, we got 70% glitch filter
- This filter was used by the logic simulator to generate gate level VCD

```
+transport_path_delays +transport_int_delays
+pulse_e/70 +pulse_int_e/70
+pulse_r/70 +pulse_int_r/70
```

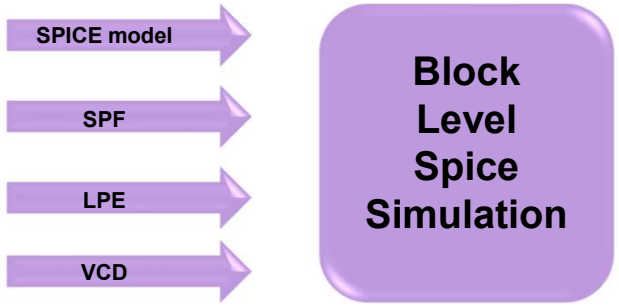
- Total power was lower than the initial result (0% filter), but still much higher than zero-delay simulation

Power Estimation

Hierarchy Level

- Starting with early power analysis, via glitch analysis in cell level, we took another step forward to estimate power in hierarchy level using *PrimeSim*:
  - Small representative sub-block (RTL -> netlist)
  - Separate logic simulation (VCD)
  - RC extraction using stdcell cdl (SPF)

```
SPICE_SUBCKT_FILE: <files> #obtain port ordering information for skip cells

NETLIST_FORMAT: SPF

NETLIST_INSTANCE_SECTION: YES
```

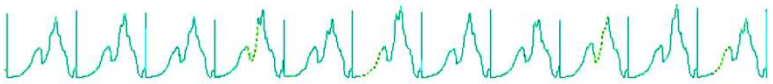


Power Estimation

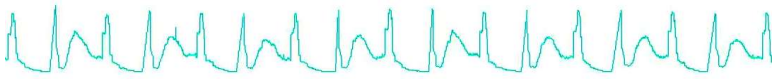
Hierarchy Level

```
.inc extracted_libcells.inc
.option search="./SPICE_MODEL/"
.temp 125
.vcd2vec file.vcd file.sig
.meas tran VDD_avg_p avg p(VDD)
.meas tran VDD_avg_p_partial avg p(VDD) from=Xns to=Yns
.meas tran VDD_max_power max p(VDD) from=Xns to=Yns
.meas tran VDD_p2p_power pp p(VDD) from=Xns to=Yns
```

PrimeSim



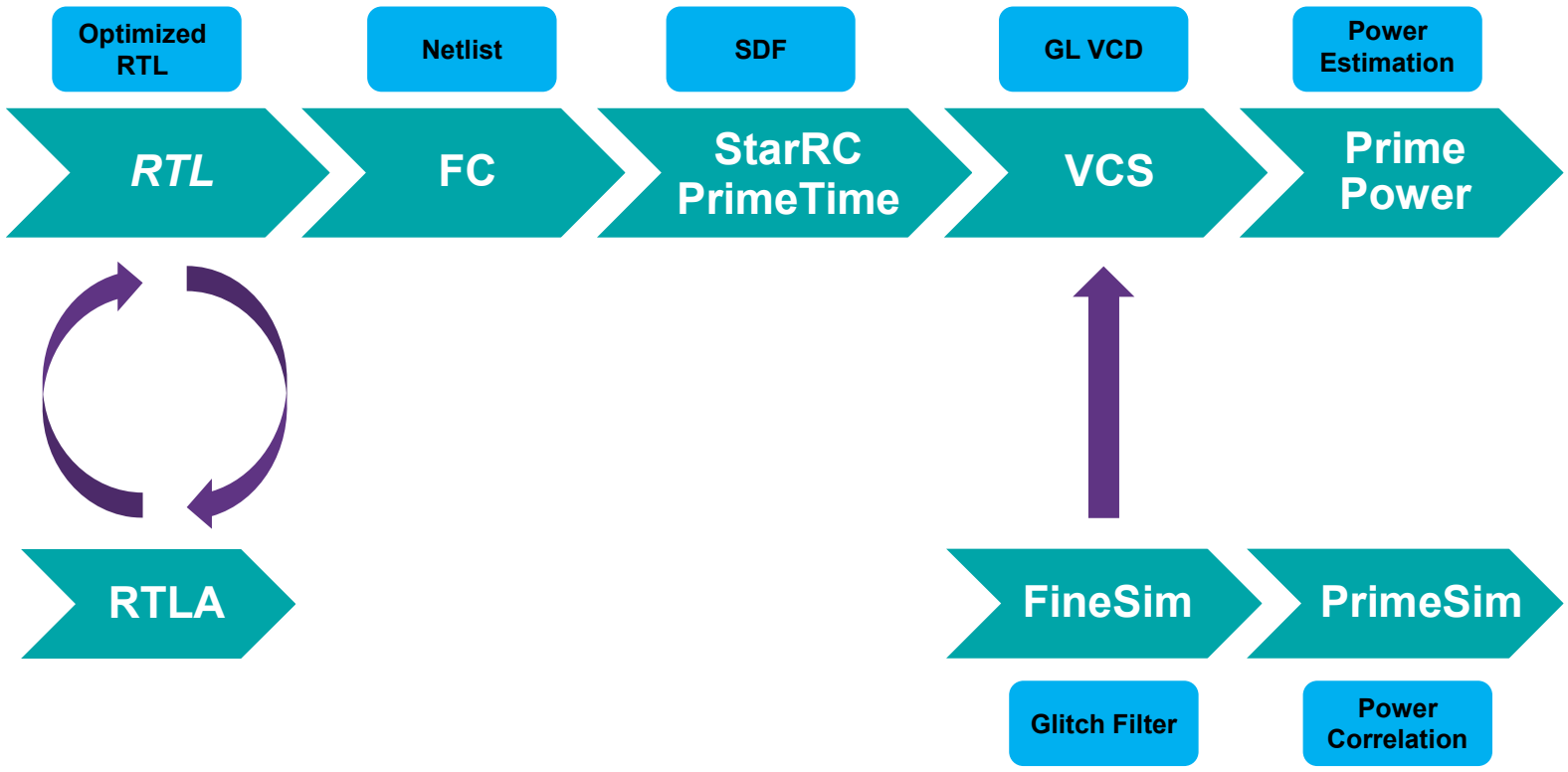
PrimePower



- Realistic simulation for custom cells evaluation
- Waveform and spike validation
- Total power estimations strongly correlate

Power Estimation

Interim Summary



Power Grid
Redhawk Fusion

Power Grid

Redhawk Fusion

- RedHawk Fusion was used for gate-level rail analysis in the power scenario, to identify major issues at early stages
- The results strongly correlate with EMIR signoff tool
- RedHawk Fusion analysis flow:
  - Import design data:

```
open_lib, open_block
```

  - Define settings:

```
set_app_options -name rail.enable_redhawk -value true
set_app_options -name rail.redhawk_path -value {}
set_app_options -name rail.tech_file –value {}
set_app_options -name rail.lib_files -value {}
set_app_options -name rail.scenario_name -value $power_scenario
set_app_options -name rail.frequency  -value {}
set_app_options -name rail.temperature  -value {}
```

Power Grid

Redhawk Fusion

- Define voltage source:

```
create_taps -import {<ploc>}
```

- Run rail analysis:

```
analyze_rail -voltage_drop $voltage_drop -nets {VDD VSS} -switching_activity \
{VCD $vcd_file $strip_path}
```

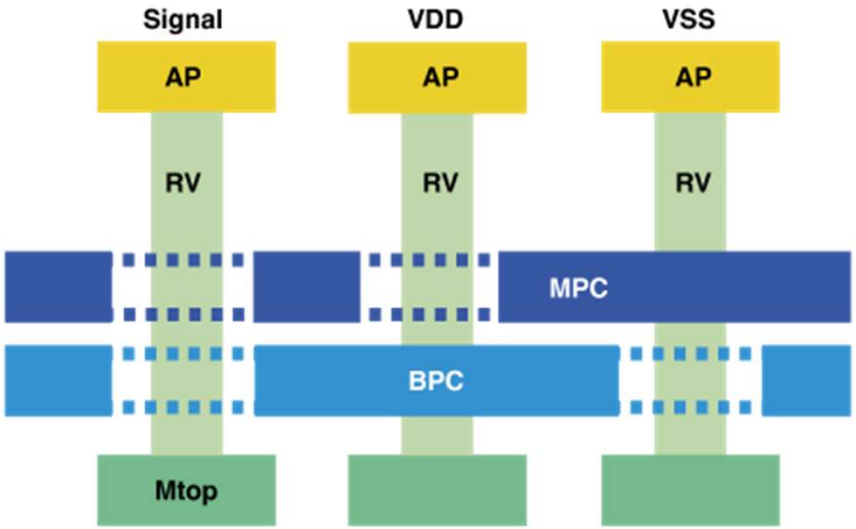
- Report:

```
report_rail_result -type effective_voltage_drop -threshold $threshold -supply_nets {VDD VSS}
```

Power Grid

MIM capacitor

- MIM capacitor insertion significantly improved grid capacitance, reducing IR drop



Post-Si Measurements

Post-Si Measurements

IR Drop

- Post-Si measurements: IR drop ≤ 2%
- IR drop inside the die is relatively low:

Layer Based Drop

Layer	**Max Drop** (%)
RDL *(including package)*	75%
M_0-M_{top}	25%

Post-Si Measurements

Power results

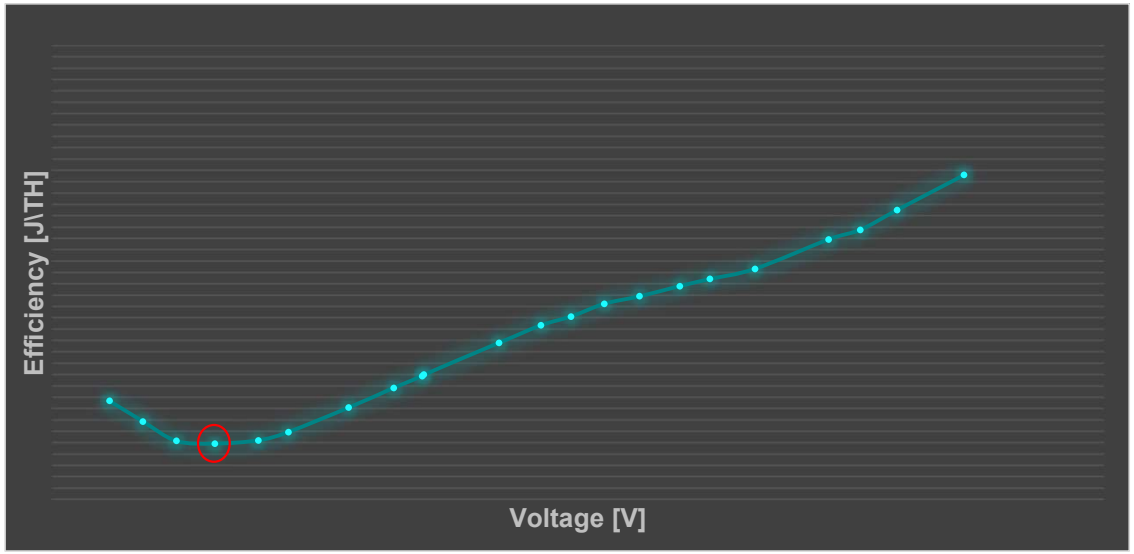
- Post-Si leakage (avg) measurements and simulated leakage power are as close as 3%

- Post-Si dynamic power measurements and simulated dynamic power are as close as 1%

Post-Si Measurements

Efficiency

- Proper function (verified by logic bist) at nominal voltage and target frequency was achieved:



Summary

Summary

- Cutting edge technology provided benefit and challenges
- Low operating voltage achieved by library re-characterization
- Early exploration reduced TAT
- Strong PnR flow allowed smooth convergence
- Glitch filter techniques applied
- Reliable power estimation
- Robust power grid
- Silicon proven methodology


THANK YOU
Our
Technology,
Your
Innovation™